IN THE CLAIMS

1. (Currently Amended) A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

doping a first region of a semiconductor substrate;

incising the substrate to provide an array of edges having substantially vertical edge surfaces, pairs of the edge surfaces facing one another ~~and spaced apart a distance equal to one half of a pitch of the array of edges~~;

doping second regions between the pairs of edge surfaces;

disposing respective structures each providing an electronic memory function on at least some respective ones of the edge surfaces, ~~the structure is composed of an oxide-nitride-oxide structure formed under a control gate such that the nitride is adapted to be a charge storage layer~~ each structure having a gate insulator formed on an edge surface and extending to a doped second region, and a control gate formed on the gate insulator; and

establishing electrical contacts to the first and second regions.

2. (Currently Amended) The method of claim 1, wherein disposing comprises:

forming ONO structures on at least some respective ones of the edge surfaces as the gate insulators; and

creating respective control gates on the ONO structures.

3. (Currently Amended) The method of claim 1, wherein disposing comprises:

forming ONO structures on at least some respective ones of the edge surfaces as the gate insulators; and

creating respective control gates on the ONO structures, wherein forming ONO structures comprises:

growing silicon dioxide from silicon comprising the edge surfaces and second regions of the substrate;

forming a silicon nitride layer on the silicon dioxide adjacent the edge surfaces; and

forming silicon dioxide on the silicon nitride.

4. (Currently Amended) The method of claim 1, wherein disposing comprises forming respective polysilicon gates ~~on respective ones of the surface edges~~ as the control gates.

5. (Currently Amended) The method of claim 1, wherein disposing comprises:
forming a first gate dielectric on ~~the~~ an edge surface ~~edge~~;
forming a ~~floating gate~~ charge trapping insulator on the first gate dielectric;
forming a second gate dielectric on the ~~floating gate~~ charge trapping insulator; and
forming a control gate on the second gate dielectric[[.]];
wherein the first gate dielectric, the charge trapping insulator and the second gate dielectric form a gate insulator.

6. (Currently Amended) The method of claim 1, wherein disposing comprises disposing structures ~~comprising gates~~ each configured to store more than one bit per ~~gate~~ memory cell.

7-8. (Canceled)

9. (Original) The method of claim 1, wherein the semiconductor substrate comprises silicon.

10. (Canceled)

11. (Currently Amended) A method for making an array of memory cells configured to store at least one bit per one F^2 comprising: ~~The method of claim 10, further comprising:~~
doping a first region of a semiconductor substrate;
incising the substrate to provide an array of substantially vertical edge surfaces, pairs of the edge surfaces facing one another ~~and spaced apart a distance equal to one half of a minimum pitch of the array of edges~~; [[and]]
doping second regions of the substrate between the pairs of edge ~~surfaces, wherein:~~ surfaces;

disposing non-horizontal structures providing an electronic memory function on the substantially vertical edge surfaces, wherein the non-horizontal structures each comprise an insulator structure having first portions formed on a pair of edge surfaces and a second portion formed on a second region between the pair of edge surfaces, and a control gate coupled to the first and second portions of the insulator structure; and

~~disposing comprises disposing the non-horizontal structures on the substantially vertical edge surfaces; and~~

establishing electrical contacts includes establishing electrical contacts to the first and second regions and to the control gates of the non-horizontal structures.

12. (Currently Amended) The method of claim 11, wherein disposing the non-horizontal structures on the substantially vertical edge surfaces comprises:

forming ONO structures on at least some of the pairs of edge surfaces; and

creating respective control gates on the ONO structures; ~~structures, wherein the structures providing the electronic memory function are configured to store more than one bit per gate.~~

wherein the ONO structures each contain an oxide layer formed on a pair of edge surfaces and on a second region between that pair of edge surfaces.

13. (Canceled)

14. (Currently Amended) The method of claim 11[[10]], wherein the structures providing the electronic memory function are configured to store more than one bit per ~~gate~~ memory cell.

15. (Currently Amended) The method of claim 11, wherein disposing non-horizontal structures comprises:

forming a first gate dielectric on a pair of the edge surfaces and a second region of the substrate between the pair of edge surfaces;

forming a ~~floating gate~~ charge trapping insulator on portions of the first gate dielectric adjacent the edge surfaces~~, wherein the floating gate is configured to store more than one bit per floating gate~~;

forming a second gate dielectric on the ~~floating gate~~ charge trapping insulator and a remaining portion of the first gate dielectric adjacent the second region; and

forming a control gate on the second gate dielectric[[.]]

wherein the first gate dielectric, the charge trapping insulator and the second gate dielectric form the insulator structure.

16. (Canceled)

17. (Currently Amended) The method of claim 11, wherein disposing comprises forming respective polysilicon gates ~~on the edge surfaces~~ as the control gates.

18. (Canceled)

19. (Currently Amended) The method of claim 11[[10]], wherein disposing comprises disposing a structure that is configured to provide an electronic memory function by storing holes.

20. (Currently Amended) The method of claim 11[[10]], wherein disposing non-horizontal structures comprises disposing substantially vertical structures.

21. (Currently Amended) A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

disposing non-horizontal structures providing an electronic memory function in trenches of a semiconductor substrate ~~spaced apart a distance equal to one half of a minimum pitch of the array~~, wherein the structures providing the electronic memory function are configured to store more than one bit per gate and are composed of an oxide-nitride-oxide (ONO) gate dielectric formed under a control gate, wherein first oxide layers of the ONO gate dielectrics are formed on

sidewalls and bottoms of the trenches, and wherein the control gates are formed on second oxide layers of the ONO gate dielectrics ~~such that the nitride is adapted to be a charge storage layer~~; and

establishing electrical contacts to memory cells including the non-horizontal structures.

22. (Original) The method of claim 21, wherein disposing non-horizontal structures comprises disposing substantially vertical structures.

23. – 112. (Canceled)